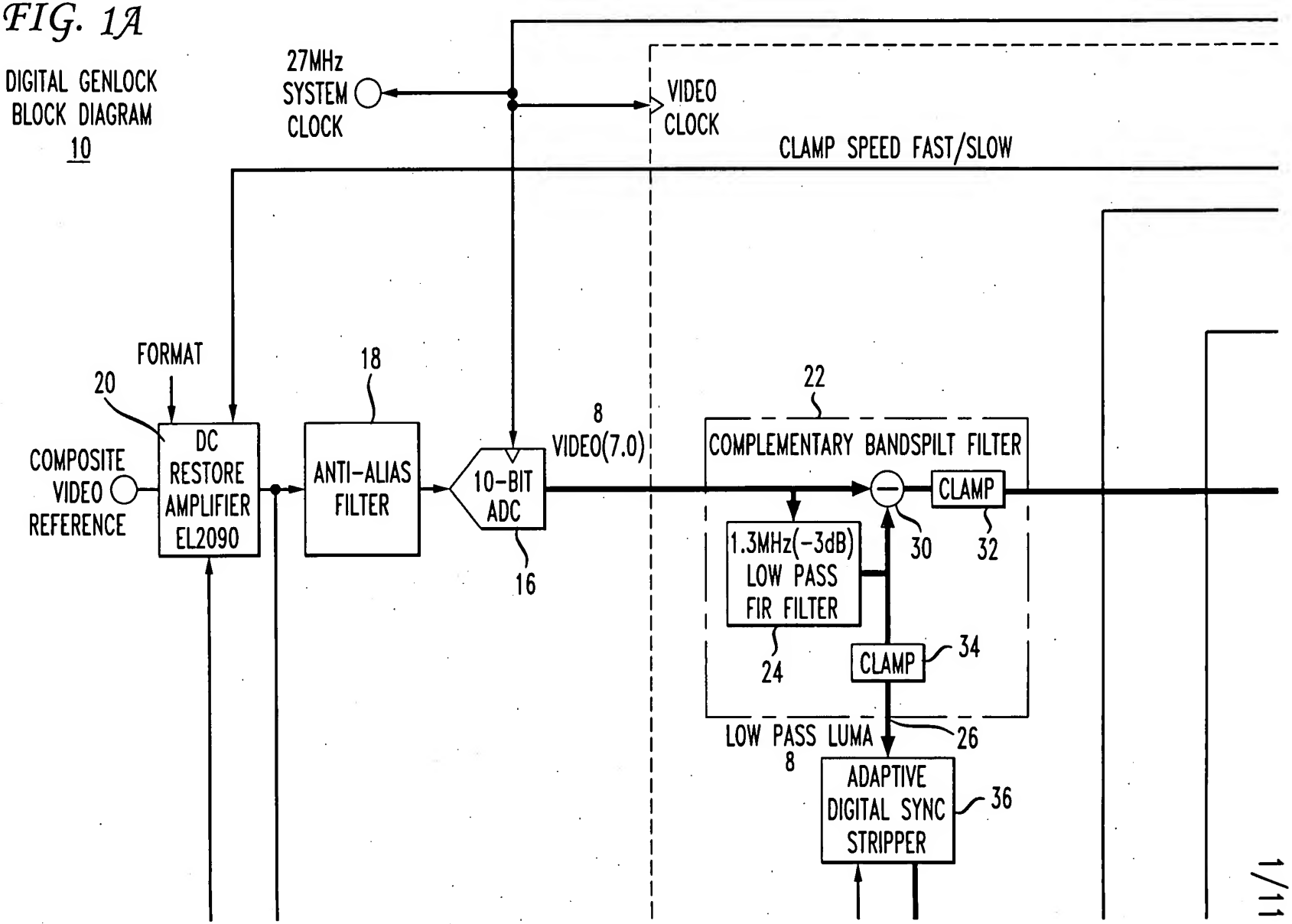
FIG. 1A


DIGITAL GENLOCK
BLOCK DIAGRAM
10
27MHz
SYSTEM
CLOCK
VIDEO
CLOCK
CLAMP SPEED FAST/SLOW
FORMAT
20
18
22
COMPOSITE
VIDEO
REFERENCE
DC
RESTORE
AMPLIFIER
EL2090
ANTI-ALIAS
FILTER
10-BIT
ADC
8
VIDEO(7.0)
COMPLEMENTARY BANDSPILT FILTER
CLAMP
1.3MHz(-3dB)
LOW PASS
FIR FILTER
30
32
16
24
CLAMP
34
LOW PASS LUMA
8
26
ADAPTIVE
DIGITAL SYNC
STRIPPER
36

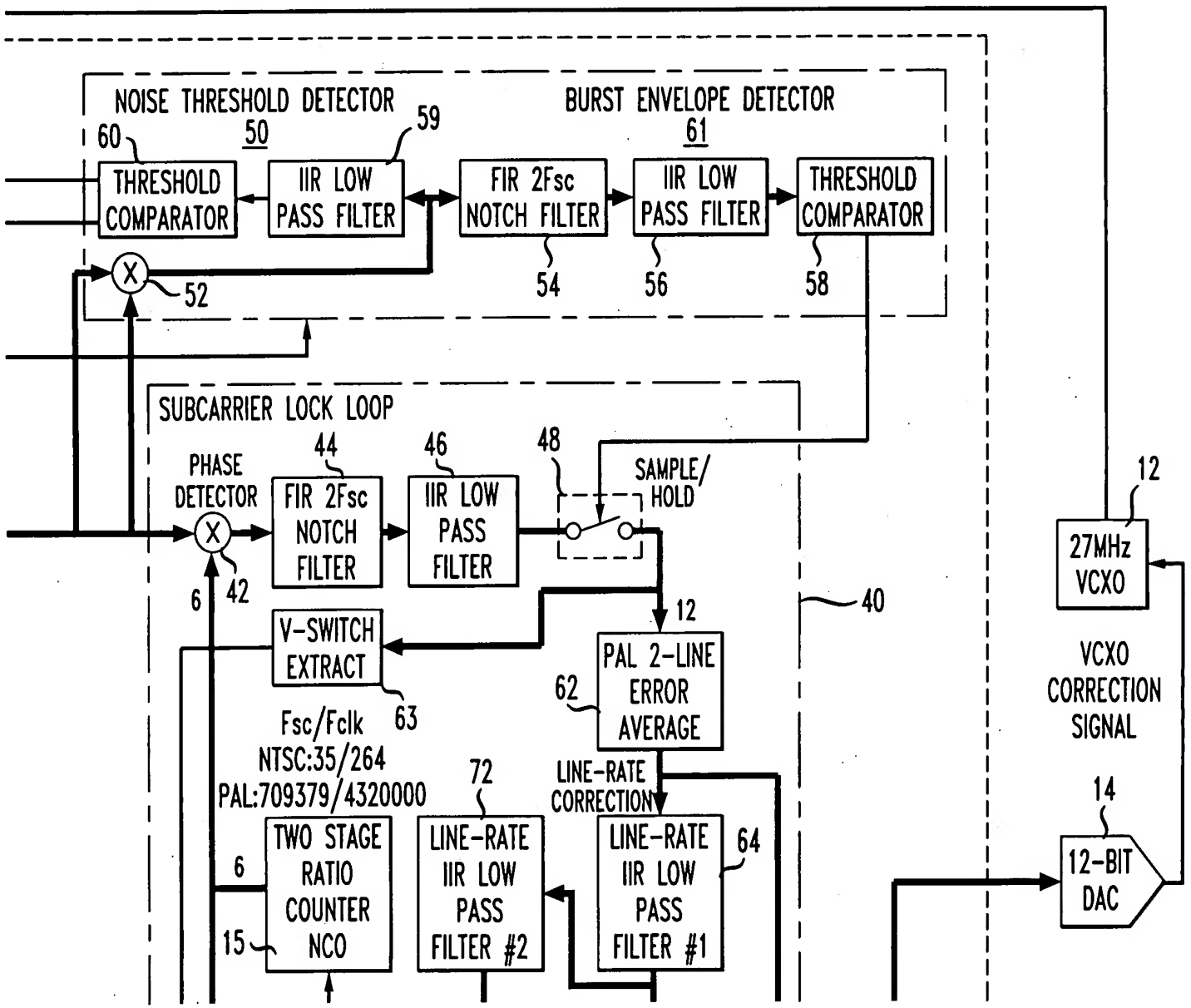


FIG. 1B

DIGITAL GENLOCK BLOCK DIAGRAM
10

FIG. 1C

DIGITAL GENLOCK
BLOCK DIAGRAM
10

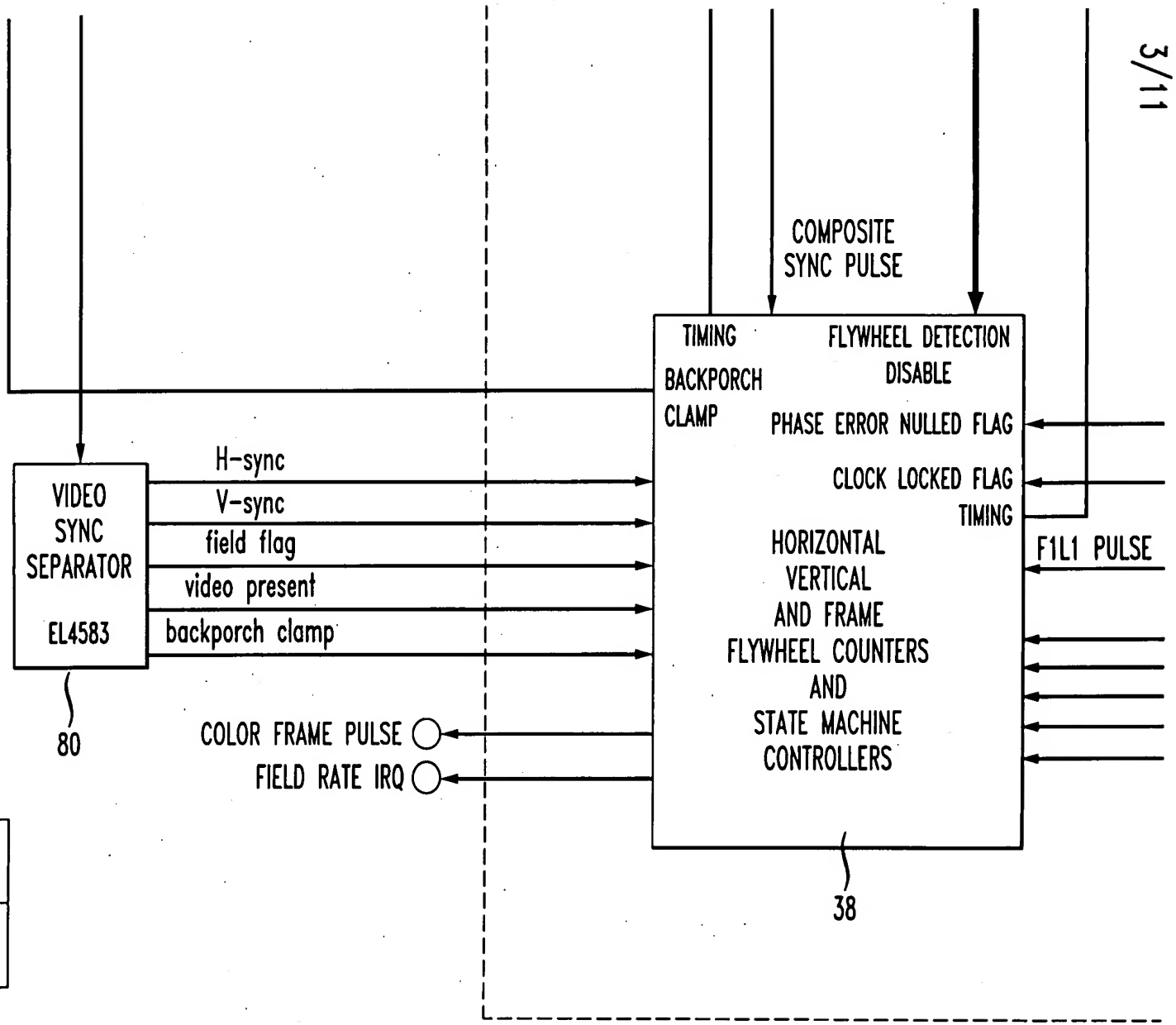


FIG. 1

FIG. 1A	FIG. 1B
FIG. 1C	FIG. 1D

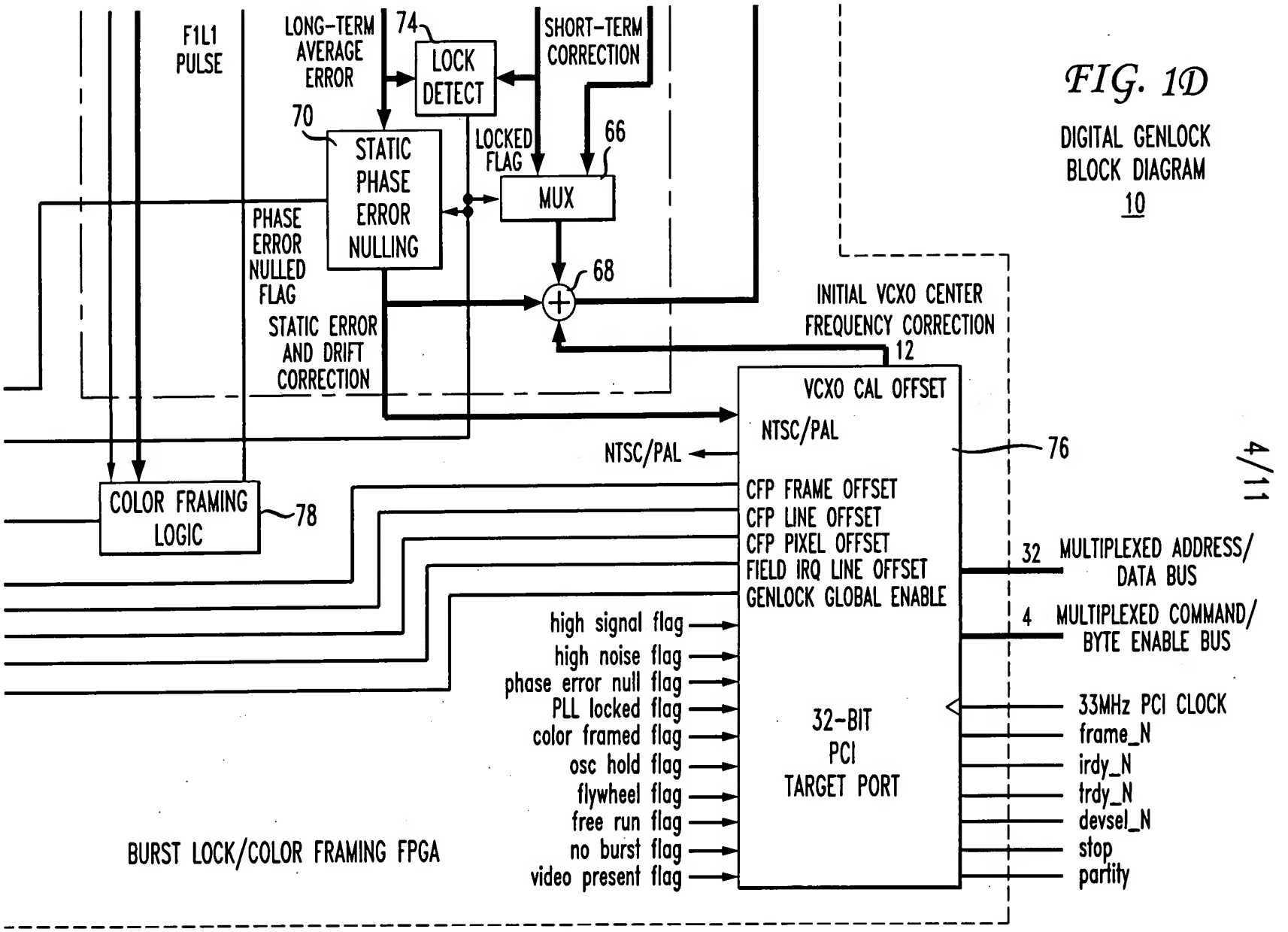


FIG. 1D

DIGITAL GENLOCK BLOCK DIAGRAM 10

FIG. 2

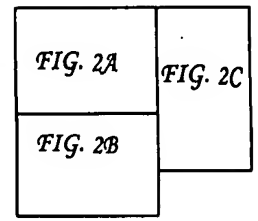
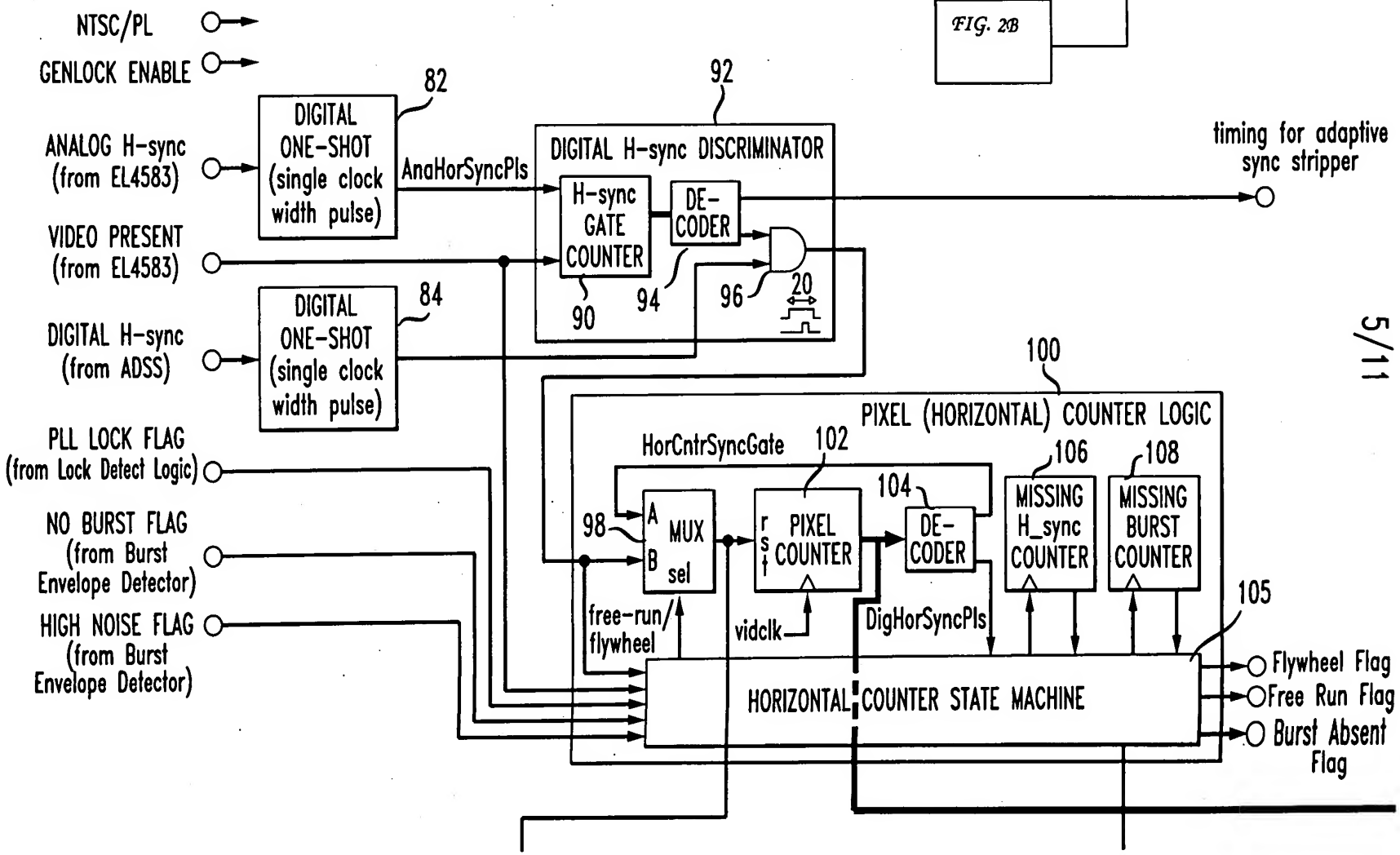


FIG. 2A
FIG. 2C
FIG. 2B

FIG. 2A


NTSC/PL
GENLOCK ENABLE
ANALOG H-sync (from EL4583)
VIDEO PRESENT (from EL4583)
DIGITAL H-sync (from ADSS)
PLL LOCK FLAG (from Lock Detect Logic)
NO BURST FLAG (from Burst Envelope Detector)
HIGH NOISE FLAG (from Burst Envelope Detector)
DIGITAL ONE-SHOT (single clock width pulse)
82
AnaHorSyncPls
DIGITAL ONE-SHOT (single clock width pulse)
84
92
DIGITAL H-sync DISCRIMINATOR
H-sync GATE COUNTER
DE-CODER
90
94
96
20
timing for adaptive sync stripper
100
PIXEL (HORIZONTAL) COUNTER LOGIC
HorCntrSyncGate
102
104
106
108
98
A
B
MUX
sel
r
s
t
PIXEL COUNTER
DE-CODER
MISSING H_sync COUNTER
MISSING BURST COUNTER
free-run/ flywheel
vidclk
DigHorSyncPls
105
HORIZONTAL COUNTER STATE MACHINE
Flywheel Flag
Free Run Flag
Burst Absent Flag

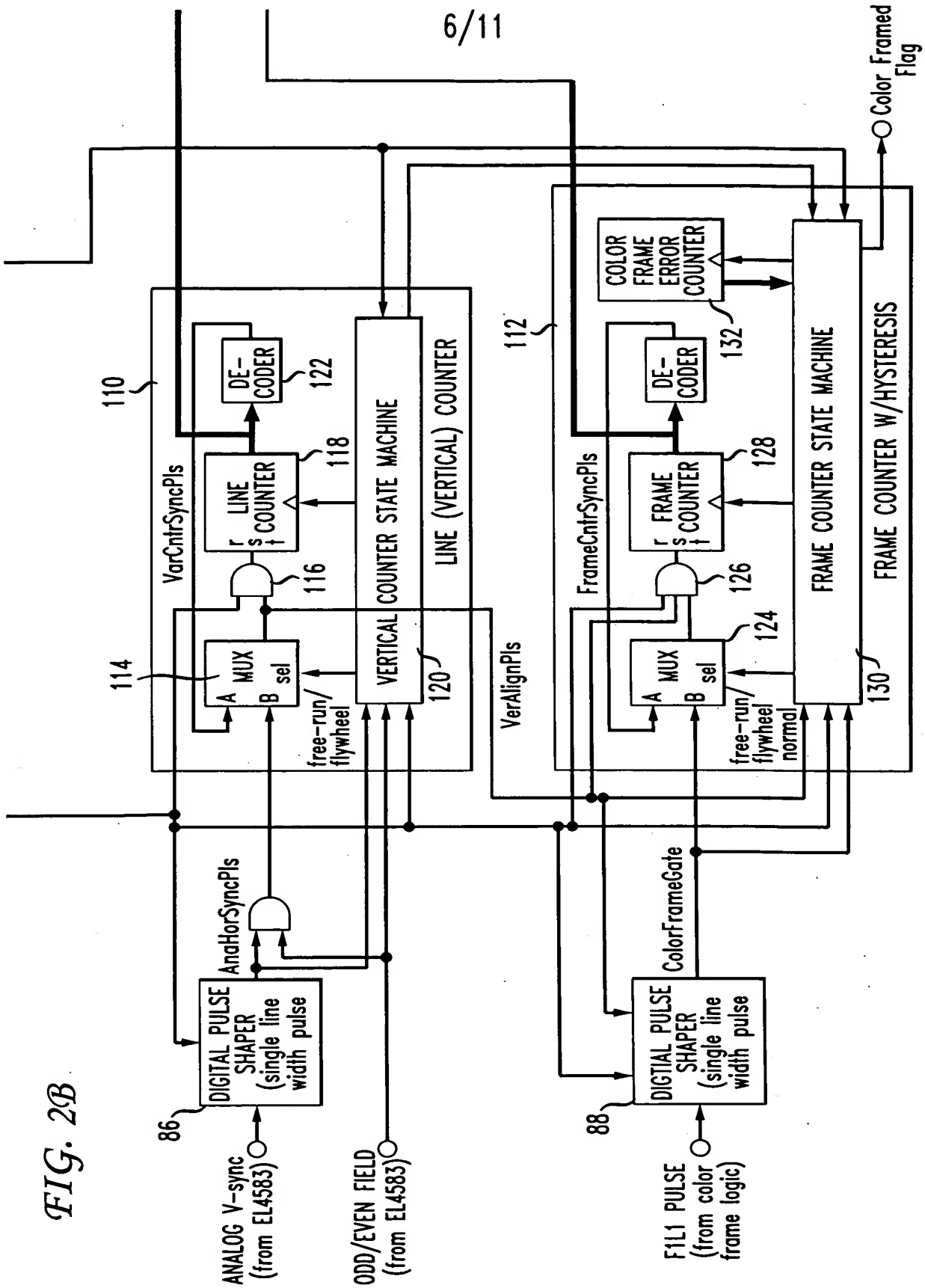

110
112
VarCntrSyncPls
FrameCntrSyncPls
DE-CODER
122
DE-CODER
132
r LINE s COUNTER t
118
r FRAME s COUNTER t
128
116
126
114
A MUX B sel
124
free-run/ flywheel
free-run/ flywheel normal
VERTICAL COUNTER STATE MACHINE
120
LINE (VERTICAL) COUNTER
VerAlignPls
COLOR FRAME ERROR COUNTER
FRAME COUNTER STATE MACHINE
130
FRAME COUNTER W/HYSTERESIS
Color Framed Flag
AnaHorSyncPls
ColorFrameGate
DIGITAL PULSE SHAPER (single line width pulse
86
88
ANALOG V-sync (from EL4583)
ODD/EVEN FIELD (from EL4583)
F1L1 PULSE (from color frame logic)

FIG. 2B

FIG. 2C

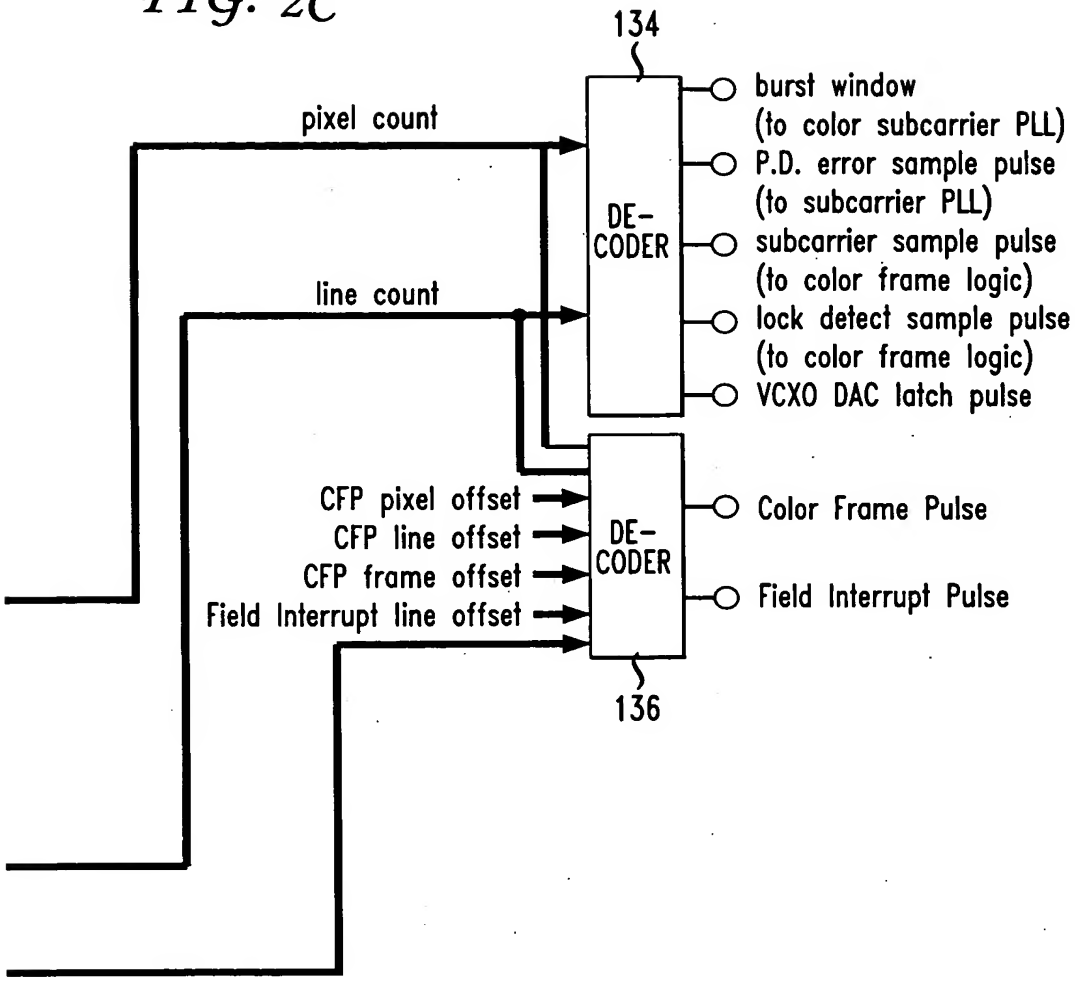

134
pixel count
line count
DE-CODER
burst window
(to color subcarrier PLL)
P.D. error sample pulse
(to subcarrier PLL)
subcarrier sample pulse
(to color frame logic)
lock detect sample pulse
(to color frame logic)
VCXO DAC latch pulse
CFP pixel offset
CFP line offset
CFP frame offset
Field Interrupt line offset
DE-CODER
Color Frame Pulse
Field Interrupt Pulse
136

FIG. 3

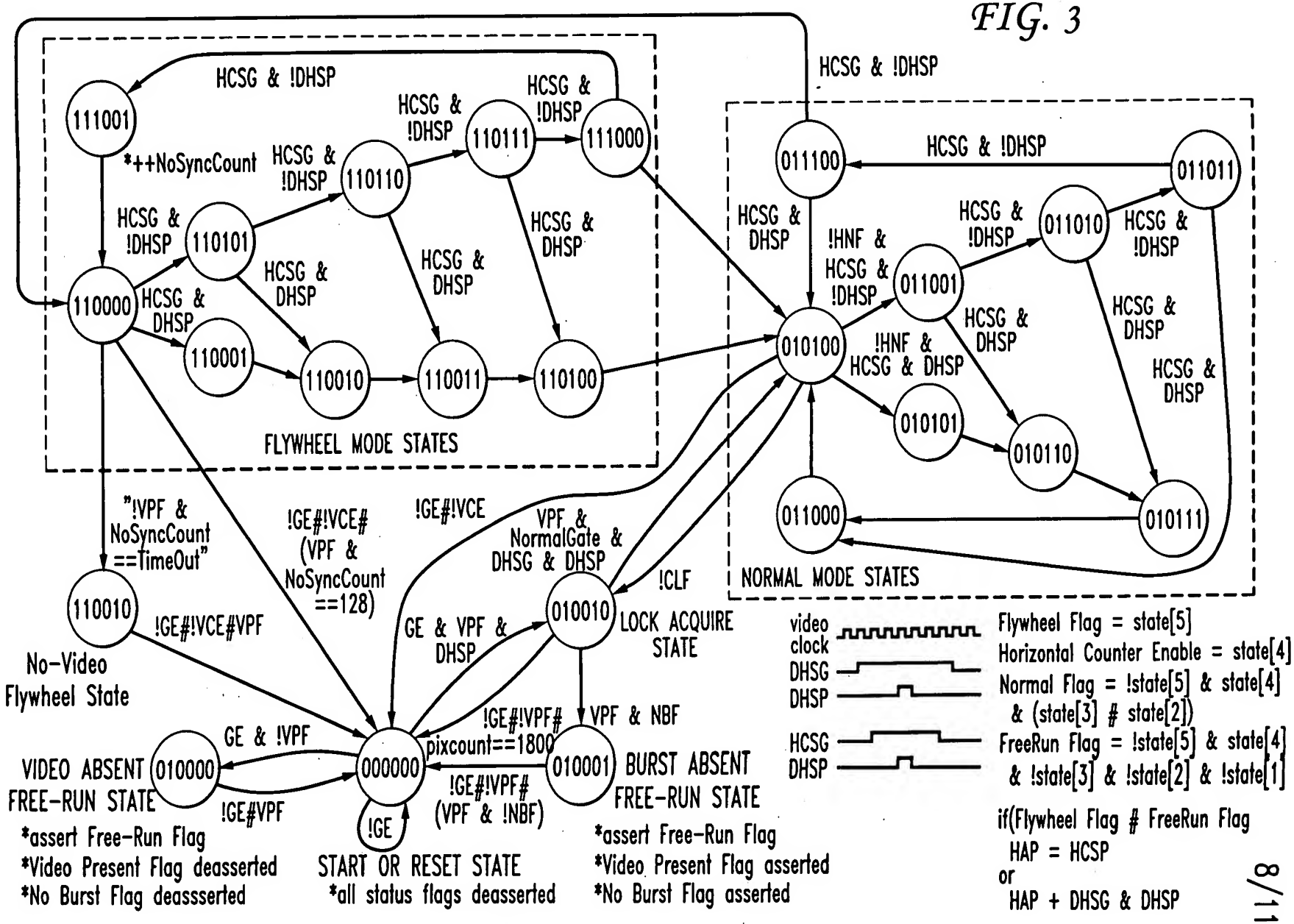
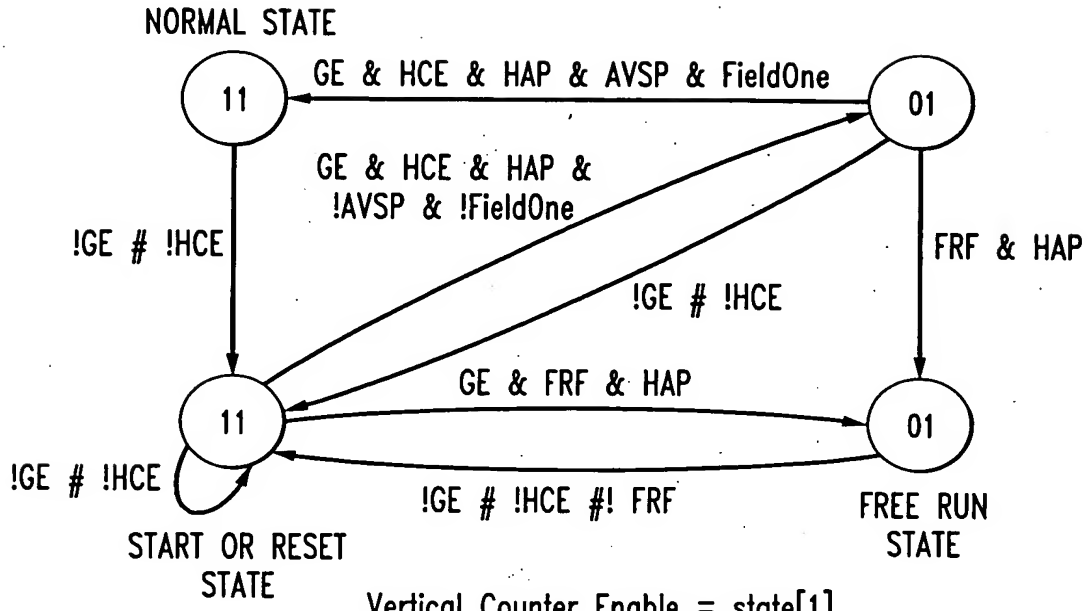

HCSG & !DHSP
111001
*++NoSyncCount
HCSG & !DHSP
110110
HCSG & !DHSP
110111
HCSG & !DHSP
111000
HCSG & !DHSP
110101
HCSG & DHSP
HCSG & DHSP
HCSG & DHSP
110000
HCSG & DHSP
110001
110010
110011
110100
FLYWHEEL MODE STATES
HCSG & !DHSP
011100
HCSG & !DHSP
011011
HCSG & DHSP
!HNF & HCSG & !DHSP
011001
HCSG & !DHSP
011010
HCSG & !DHSP
HCSG & DHSP
010100
!HNF & HCSG & DHSP
HCSG & DHSP
HCSG & DHSP
HCSG & DHSP
010101
010110
011000
010111
NORMAL MODE STATES
"!VPF & NoSyncCount ==TimeOut"
!GE#!VCE# (VPF & NoSyncCount ==128)
!GE#!VCE
VPF & NormalGate & DHSG & DHSP
!CLF
110010
!GE#!VCE#VPF
No-Video Flywheel State
GE & VPF & DHSP
010010
LOCK ACQUIRE STATE
!GE#!VPF# pixcount==1800
VPF & NBF
GE & !VPF
VIDEO ABSENT FREE-RUN STATE
010000
000000
010001
BURST ABSENT FREE-RUN STATE
!GE#VPF
!GE#!VPF# (VPF & !NBF)
!GE
*assert Free-Run Flag
*Video Present Flag deasserted
*No Burst Flag deassserted
START OR RESET STATE
*all status flags deasserted
*assert Free-Run Flag
*Video Present Flag asserted
*No Burst Flag asserted
video clock
DHSG
DHSP
HCSG
DHSP
Flywheel Flag = state[5]
Horizontal Counter Enable = state[4]
Normal Flag = !state[5] & state[4] & (state[3] # state[2])
FreeRun Flag = !state[5] & state[4] & !state[3] & !state[2] & !state[1]
if(Flywheel Flag # FreeRun Flag
HAP = HCSP
or
HAP + DHSG & DHSP

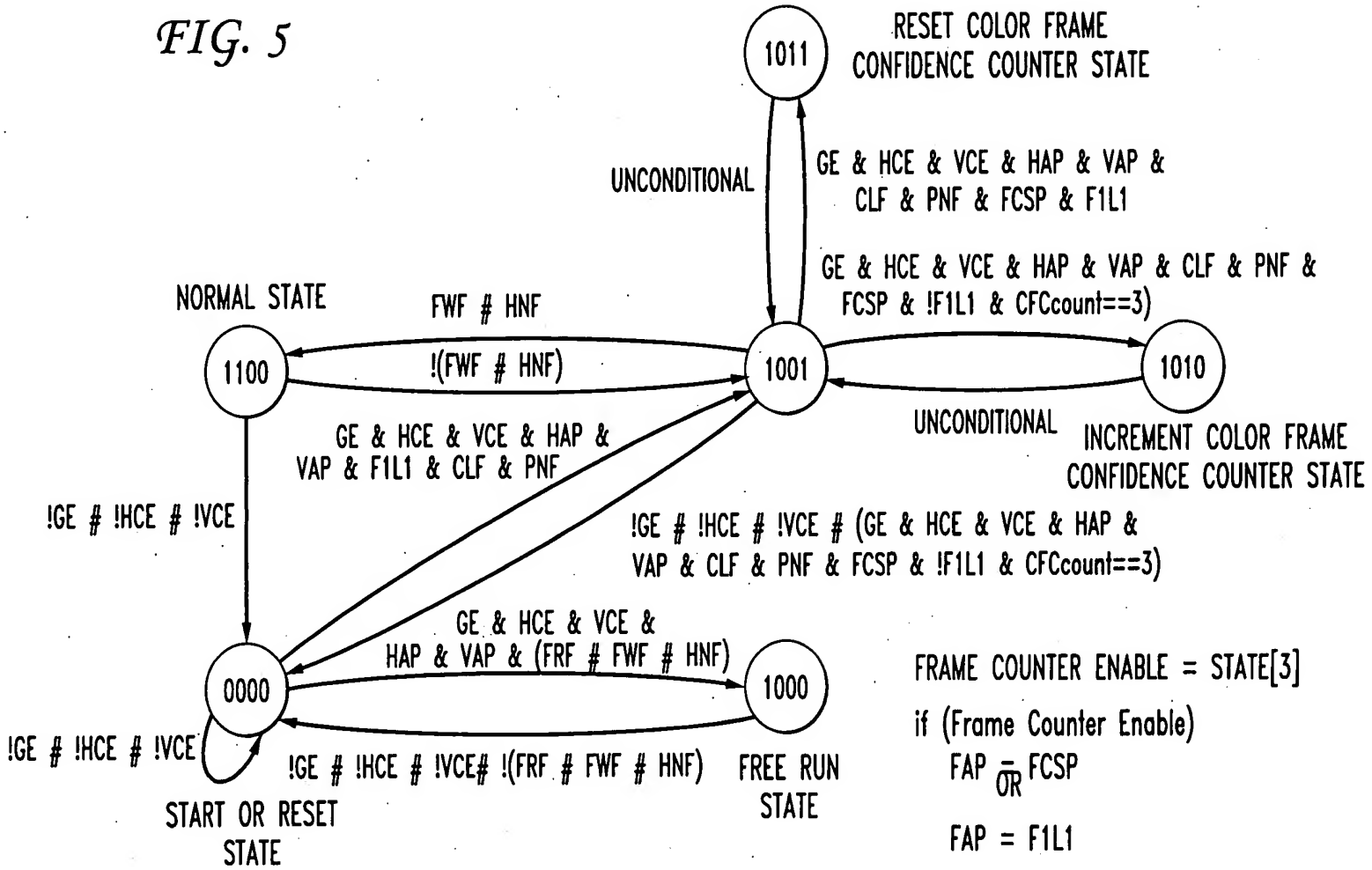
FIG. 4



Vertical Counter Enable = state[1]

if (Normal Flag # Flywheel Flag # FreeRun Flag)
VAP = VCSP
OR
VAP = AVSP & FieldOne

FIG. 5


1011
RESET COLOR FRAME CONFIDENCE COUNTER STATE
UNCONDITIONAL
GE & HCE & VCE & HAP & VAP & CLF & PNF & FCSP & F1L1
GE & HCE & VCE & HAP & VAP & CLF & PNF & FCSP & !F1L1 & CFCcount==3)
NORMAL STATE
FWF # HNF
1100
!(FWF # HNF)
1001
1010
UNCONDITIONAL
INCREMENT COLOR FRAME CONFIDENCE COUNTER STATE
GE & HCE & VCE & HAP & VAP & F1L1 & CLF & PNF
!GE # !HCE # !VCE
!GE # !HCE # !VCE # (GE & HCE & VCE & HAP & VAP & CLF & PNF & FCSP & !F1L1 & CFCcount==3)
GE & HCE & VCE & HAP & VAP & (FRF # FWF # HNF)
0000
1000
!GE # !HCE # !VCE
!GE # !HCE # !VCE# !(FRF # FWF # HNF)
START OR RESET STATE
FREE RUN STATE
FRAME COUNTER ENABLE = STATE[3]
if (Frame Counter Enable)
FAP = FCSP
OR
FAP = F1L1

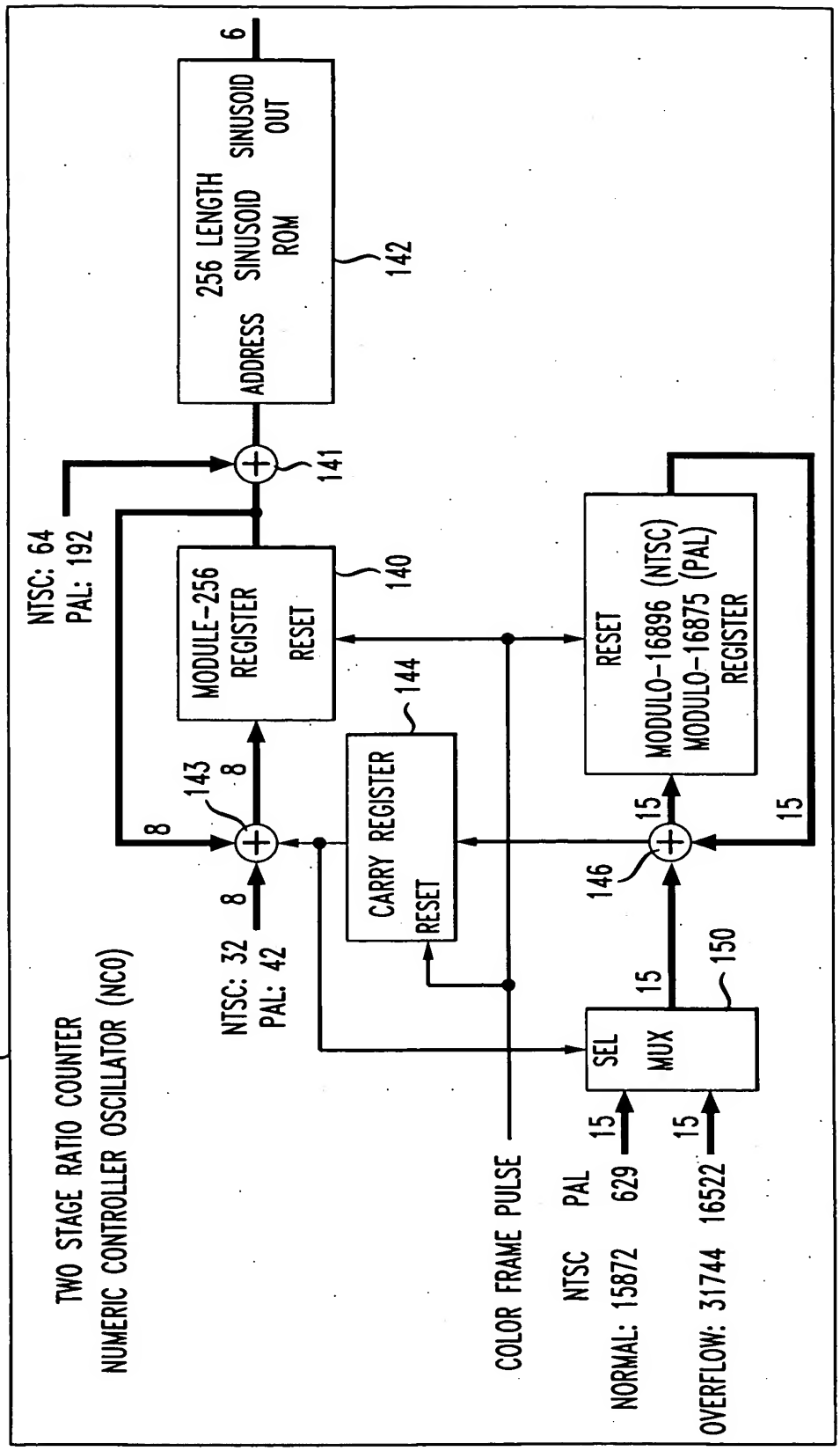

15
TWO STAGE RATIO COUNTER
NUMERIC CONTROLLER OSCILLATOR (NCO)
256 LENGTH SINUSOID ROM
ADDRESS
SINUSOID OUT
6
142
141
NTSC: 64
PAL: 192
MODULE-256 REGISTER
RESET
140
143
8
8
8
NTSC: 32
PAL: 42
CARRY REGISTER
RESET
144
RESET
MODULO-16896 (NTSC)
MODULO-16875 (PAL)
REGISTER
15
15
146
SEL
MUX
15
150
15
COLOR FRAME PULSE
NTSC PAL
NORMAL: 15872 629
OVERFLOW: 31744 16522

FIG. 6